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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/830,092	06/27/2001	Kazutaka Shibata	ROH-037	1091

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EXAMINER	
SONG, MATTHEW J	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 12/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/830,092	SHIBATA, KAZUTAKA	
	Examiner	Art Unit	
	Matthew J Song	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 10-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Sekine et al (WO99/09595), where US 6,495,914 is used as an accurate translation and an accurate translation can be provided upon request.

Sekine et al discloses bare chip devices **47** each including a plurality of semiconductor devices or IC chips with metal bumps **46** provided on the electrodes are placed and bonded on a base substrate **41** this reads on applicant's chip bonding step. Sekine et al also discloses connection posts (projections) **42** connected to electrodes **44** formed by etching, this reads on applicant's electrode forming step. Sekine et al also discloses epoxy resin **48** is filled in the recesses on the base substrate and coated over the projections and bare chip devices. The epoxy resin is flattened in its surface by grinding or polishing so that the connection posts **42,** and the metal bumps on the bare chip devices can be exposed, this reads on applicant's resin sealing step. Sekine et al also discloses the base substrate with module structures is cut along the centers between the adjacent surrounding walls into individual multi-chip module structures, this reads on applicant's cutting step ('914 col 9, ln 1-55 and Figs 4a-4d). Sekine et al also discloses

Referring to claim 10, Sekine et al discloses a bare chip device **47,** including a plurality of semiconductor devices or IC chips bonded on a base substrate **41**, this reads on applicant's semiconductor chip bonded to the solid device. Sekine et al also discloses projections **42** and electrodes **44**, this reads on applicant's projection electrodes, and a epoxy resin coated over the projections and chips ('914 col 6, ln 5-40).

Referring to claims 11-12 and 14, Sekine et al discloses a plurality of chips and the semiconductor chip is bonded face down onto the solid device with an active surface of the semiconductor chip opposed to the solid device and substrate ('914 Figs 4a-4d).

Referring to claim 13, Sekine et al discloses a substrate **41**.

Referring to claims 15-16, Sekine et al discloses the electrodes can be drawn directly out of the rear side of the substrate and conductive holes **54** ('914 col 6, ln 30-55 and Figs 4a-4d)

Referring to claims 18-19, Sekine et al discloses grinding the resin to expose the chip devices and projections ('914 col 6, ln 20-30), this reads on applicant's removing a surface layer section of the resin.

Referring to claim 20, Sekine et al discloses the rear side of the multi-chip module strucure is ground by grinding prior to the cutting step (col 6, ln 35-45).

Referring to claim 21, Sekine et al discloses the projection electrodes 42 are formed to be higher than the active surface of the semiconductor chip **46** and lower than the inactive surface of the semiconductor chip (Figs 4a-4d).

Referring to claim 22-23, Sekine et al discloses bare chip devices **47** each including a plurality of semiconductor devices or IC chips with metal bumps **46** provided on the electrodes are placed and bonded on a base substrate **41** this reads on applicant's chip bonding step of

bonding a chip with an active surface thereof opposed to the surface of the substrate. Sekine et al also discloses connection posts (projections) **42** connected to electrodes **44** formed by etching, this reads on applicant's electrode forming step. Sekine et al also discloses epoxy resin **48** is filled in the recesses on the base substrate and coated over the projections and bare chip devices. The epoxy resin is flattened in its surface by grinding or polishing so that the connection posts **42,** and the metal bumps on the bare chip devices can be exposed (Fig 4c), this reads on applicant's resin sealing step. Sekine et al also discloses the base substrate with module structures is cut along the centers between the adjacent surrounding walls into individual multi-chip module structures, this reads on applicant's cutting step ('914 col 9, ln 1-55 and Figs 4a-4d).

Referring to claim 24, Sekine et al discloses the electrodes can be directly drawn out of the rear side of the substrate, therefore can be soldered directly to a motherboard ('914 col 6, ln 35-55), this reads on applicant's enabling an electrical connection from a back side of the substrate.

Referring to claim 25, Sekine et al discloses the epoxy resin is flattened in its surface by grinding or polishing so that the connection posts **42,** and the metal bumps on the bare chip devices can be exposed (Fig 4c), this reads on applicant's resin sealing step.

3. Claims 10-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Egawa (JP 08-236692), where an English abstract and an English Computer translation (CT) have been provided; an accurate English Translation can be provided upon request.

Egawa discloses a hybrid intrgrated circuit device, this reads on applicant's solid device, a semiconductor chip **16, 17** bonded onto a surface of the solid device, projection electrodes for

external connection formed on the surface of the solid device **15**, and a protective resin layer **18,19** for sealing the surface of the solid device with head portions of the projection electrodes thereon exposed.

Referring to claim 11, Egawa discloses at least one semiconductor chip (CT [0014]), this reads on applicant's another semiconductor chip.

Referring to claims 12 and 14, Egawa discloses the semiconductor chip is bonded face down onto the solid device with an active surface of the semiconductor chip opposed to the solid device and substrate (Figs 1-4).

Referring to claim 13, Egawa disclose a wiring substrate (CT [0018]).

Referring to claim 15-16, Egawa discloses holes **13** provided right below the projection electrodes **23** enabling connection from the back side to the electrodes (CT [0031]-[0032]).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 3-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sekine et al (WO99/09595), where US 6,495,914 is used as an accurate translation and an accurate translation can be provided upon request, in view of Fukasawa et al (US 6,455,920) and Ichikawa (JP 02-031437), where an English Abstract has been provided and an accurate translation can be provided upon request.

Sekine et al discloses all of the limitations of claim 1, as discussed previously, except a step for forming a back side resin layer on a back side of the semiconductor substrate.

In a method of forming a semiconductor device, Fukasawa et al teaches a semiconductor device **20A** with a resin layer **41** provided on the rear surface of the semiconductor chip. Fukasawa et al teaches the semiconductor chip is improved and problem damages in the bottom surface of the chip at the time of dicing the semiconductor wafer **51** into individual chips is eliminated (col 17, ln 35 to col 18, ln 67 and Figs 23-26). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify to modify Sekine et al with Fukasawa et al's resin layer on the bottom of the chip to eliminate damage to the bottom of the semiconductor chip during dicing.

The combination of Sekine et al and Fukasawa et al does not teach a back side grinding step of thinning the semiconductor substrate by removing the back side resin through polishing or grinding, from the semiconductor substrate.

In a method of packing a semiconductor chip, Ichikawa teaches a semiconductor chip is sealed in resin **21** and the rear side of the chip is subjected to grinding for a reduction in the packaging height. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify to modify the combination of Sekine et al and Fukasawa et al with Ichikawa's grinding of a resin layer to reduce the height and enhance the packaging density.

Referring to claim 3, the combination of Sekine et al, Fukasawa et al and Ichikawa teaches a step of forming a surface resin layer **48** ('914), a back side resin layer **41** ('920) and a back side grinding step ('437) and further polishing the back side of the semiconductor ('914 col 6, ln 35-40). It is also noted that further polishing is not patentable because splitting of one step into two, where the processes are substantially identical or equivalent in terms of function, manner and result was held to be not patentably distinguish the processes (Ex Parte Rubin 128 USPQ 159).

Referring to claim 4, the combination of Sekine et al, Fukasawa et al and Ichikawa teaches cutting the substrate after grinding ('914, col 6, ln 30-45).

Referring to claim 5, the combination of Sekine et al, Fukasawa et al and Ichikawa teaches forming projections **43** ('914).

Referring to claim 6, the combination of Sekine et al, Fukasawa et al and Ichikawa the projections are embedded in the resin layer ('914 col 6, ln 5-40 and Figs 4a-4d).

Referring to claim 7, the combination of Sekine et al, Fukasawa et al and Ichikawa teaches grinding or polishing ('914 col 6, ln 20-30).

Referring to claim 8, the combination of Sekine et al, Fukasawa et al and Ichikawa is silent to the order of processing steps. The transposition of process steps where the processes are

substantially identical or equivalent in terms of function, manner and result was held to be not patentably distinguish the processes (Ex Parte Rubin 128 USPQ 159).

Referring to claim 9, the combination of Sekine et al, Fukasawa et al and Ichikawa is silent to the surface resin and the backside resin are substantially the same thickness. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Sekine et al, Fukasawa et al and Ichikawa by optimizing the thickness of the resin layer by conducting routine experimentation to obtain same.

Response to Arguments

6. Applicant's arguments with respect to claims 3-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takebashi et al (JP 59-092536) teaches applying a resin to a substrate and polishing (Abstract).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J Song whose telephone number is 703-305-4953. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 703-305-2667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

Matthew J Song
Examiner
Art Unit 1765

MJS

NADINE G. NORTON
PRIMARY EXAMINER
SUPERVISOR